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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,144	09/16/2003	Bryan D. Sheffield	TI-35286	2156

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,144	SHEFFIELD ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

10/4/06
STEPHEN C. ELMORE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed August 11, 2006 in response to the PTO Office Action mailed May 12, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1 and 11 have been amended, claim 17 has been cancelled, and no new claims have been added. Claims 1-16 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al (US Patent No. 5,239,639), Kim et al (US PGPub No. 20020054527) and Schmitt (US Patent No. 5,587,675).

For claim 1, Fischer discloses a method of operating a memory at a maximum rate, comprising:

initiating a first memory operation (upon request from the CPU, a state tracker notifies memory controller of a CPU read/write memory cycle request, col. 4, lines 54-56);

identifying a completion of the memory operation (the cycle length feedback value indicates the quantity of wait states necessary to complete the memory cycle, col. 3 lines 16-18 and col. 4, lines 56-62);

generating a cycle ready strobe signal upon the identified completion (the state tracker is able to generate a ready signal to the CPU at the end of the memory cycle, col. 4 lines 60-61);

employing the cycle ready strobe signal for initiation of a next memory operation (the CPU makes read or write cycle requests of the memory controller, such cycles are initiated when the CPU sends a cycle "start" indicator to the state tracker, col. 2 lines 65-67);

enabling selected row and column decoder circuitry for addressing one or more selected memory cells within the memory based on the transition of the internal memory clock signal (a memory controller maps memory addresses across rows then down

columns via row and column address strobes, and that the assertion of a row address strobe requires a precharge time delay to occur prior to the strobe, col. 5, lines 12-22);

initiating a tracking circuit that waits a predetermined tracking time associated with a time needed for selected true and complementary bit lines associated with the one or more selected memory cells, the initiation of the tracking circuit based on the transition of the internal memory clock signal (a control interface state tracker is connected to the memory controller and requires use of the CPU clock, and is responsible for tracking the CPU bus cycles and returning a "ready" indication back to the CPU after the memory cycle has been completed or accepted, and is also responsible for generation of timing control signals or for triggering another functional logic unit that performs the generation of the timing control signals, col. 2, lines 50-63; the state tracker returns a ready indication to the CPU after the cycle length time has been satisfied as indicated by a cycle length feedback, col. 3, lines 19-21); and

outputting a reset signal from the tracking circuit after the predetermined tracking time, thereby disabling the internal memory clock signal, and initiating a bit line precharge operation (col. 2, lines 50-63; col. 3, lines 19-21).

Fischer fails to disclose the remaining claim limitations.

Kim, however, helps disclose the following:

triggering a transition of an internal memory clock signal (when the clock signal makes a low to high transition, the selection signal is enabled synchronously, while simultaneously the precharge control signal is disabled, the selection signal is enabled and the data stored in a register is transferred to a data line, par. 0026);

transitioning a bit line precharge signal to disable a bit line precharge operation based on the transition of the internal memory clock signal (par. 0026);

establishing a voltage differential between selected true and complementary bit lines based on a state of the one or more selected memory cells (during circuit operation, one of the selection signals is selected, and selection occurs by controlling the voltages, par. 0006).

Fischer, Kim and Schmitt are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include transitioning a clock signal because this would allow for operation even at a low operation voltage and causes no voltage drop (par. 0028), as taught by Kim.

The combined teachings of Fischer, Kim and Schmitt fail to disclose outputting a reset signal from the tracking circuit, thereby disabling the internal memory clock signal.

Schmitt, however, helps disclose a multi-clock controller circuit (abstract), including a reset signal in the active state that disables any internal clock pulses (col. 3, lines 44-46).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Fischer and Schmitt to include a reset signal, thereby disabling an internal memory clock signal, because this would allow system clocks to be turned off and on in an orderly fashion (col. 1, lines 10-12), as taught by Schmitt.

For claim 2, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 1 above.

Fischer further helps disclose the memory operation comprises a read operation (col. 4, lines 54-56).

For claim 3, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 1 above.

Fischer further helps disclose the initiating a memory operation comprises:

inputting a clock strobe signal associated with a system clock signal into a memory control circuit operable to generate one or more memory control signals upon receipt of the clock strobe signal (once a cycle start indicator has been detected from the CPU, the state tracker activates a start strobe to the memory controller to start the actual memory cycle, the memory controller generates the necessary DRAM timing control signals through use of its own timing elements or integrated delay lines which are independent of the CPU clock, col. 2 lines 66-67, col. 3 lines 1-6).

For claim 4, the combined teachings of Fischer, Kim and Shmitt disclose the invention as per rejection of claim 3 above.

Fischer further helps disclose one of the control signals comprises a bit line precharge enable signal (the assertion of the row address strobe requires a precharge time delay to occur prior to the strobing of the row, col. 5 lines 18-22), and wherein generating the cycle ready strobe signal comprises activating a cycle ready circuit when the bit line precharge enable signal transition to indicate initiation of a bit line precharge operation (col. 5 lines 18-22).

For claim 5, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 4 above.

Fischer further helps disclose the activating the cycle ready circuit causes the cycle ready circuit to generate the cycle ready strobe signal a predetermined time after the bit line precharge enable signal transition (examples of different types of memory cycles include a read or write access, a page hit or page miss cycle, or a row miss cycle, each of these types of cycles has a deterministic number of clock pulses or wait states necessary to complete the cycle, col. 6 lines 2-7; the exact length of each cycle, i.e. the number of clock pulses or wait states necessary to complete the cycle, is predetermined, col. 6 lines 60-62).

For claim 6, the combined teachings of Fischer, Kim and Schmitt disclose disclose the invention as per rejection of claim 5 above.

Fischer further helps disclose the predetermined time is sufficient to ensure that one or more true and complement bit line pairs substantially equalize and reach a predetermined precharge level (once the state tracker receives information from the memory controller regarding the quantity of wait states required for the memory cycle, the state tracker delays for the specified number of wait states then sends a ready signal to the CPU at the completion of the memory cycle, thus, the ready signal is sent to the CPU at the exact moment the memory cycle finishes thereby incurring no synchronization penalty, col. 7 lines 7-15).

For claim 9, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 1 above.

Fischer further helps disclose the employing the cycle ready strobe signal for initiation of the next memory operation comprises:

identifying the generation of the cycle ready strobe signal (the ready signal is transmitted from state tracker to CPU over a line, col. 8 lines 23-25);

modifying a multiplexer input select control signal in response thereto (external control interface state tracker, fig. 1 item 300; the state tracker monitors CPU bus cycles and initiates read/write memory access cycles when requested by the CPU, col. 4 lines 51-54);

feeding a memory multiplexer logic circuit with both the clock strobe signal and the cycle ready strobe signal (fig. 1 items 300, 510, 210, 320); and

using the modified multiplexer input select control signal to pass the cycle ready strobe signal to a memory control circuit to generate one or more memory control signals for initiating the next memory operation (fig. 1 items 300, 310, 100).

For claim 11, the combined teachings of Fischer, Kim and Schmitt are incorporated herein.

These teachings further help disclose a method of operating a memory, comprising:

initiating a first memory operation with an input clock signal associated with a system clock (Fischer: col. 4, lines 54-56; the state tracker requires use of the CPU clock and is responsible for tracking CPU bus cycles and returning a ready indication back to the CPU after the memory cycle has been completed or accepted, col. 2, lines 54-59);

generating a cycle ready strobe signal upon a completion of a memory operation (col. 4 lines 60-61);

using the cycle ready strobe signal to initiate a next memory operation (col. 2 lines 65-67);

wherein initiating the first memory operation or initiating the next memory operation comprises:

triggering a transition of an internal memory clock signal (Kim: par. 0026);

transitioning a bit line precharge signal to disable a bit line precharge operation based on the transition of the internal memory clock signal (par. 0026);

enabling selected row and column decoder circuitry for addressing one or more selected memory cells within the memory based on the transition of the internal memory clock signal (col. 5, lines 12-22);

initiating a tracking circuit that waits a predetermined tracking time associated with a time needed for selected true and complementary bit lines associated with the one or more selected memory cells to establish a voltage differential therebetween based on a state of the one or more selected memory cells, the initiation of the tracking circuit based on the transition of the internal memory clock signal (Kim: par. 0006; Fischer: col. 2, lines 50-63; col. 3, lines 19-21); and

outputting a reset signal from the tracking circuit after the predetermined tracking time, thereby disabling the internal memory clock signal, and initiating a bit line precharge operation (Schmitt: abstract; col. 3, lines 44-46).

For claim 12, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 11 above.

Fischer further helps disclose the cycle ready strobe signal transitions to enable initiation of the next memory operation a predetermined period of time after the completion of the memory operation (col. 6 lines 60-62; once the state tracker receives information from the memory controller regarding the quantity of wait states required for the memory cycle, the state tracker delays for the specified number of wait states then sends a ready signal to the CPU at the completion of the memory cycle, col. 7 lines 7-15).

6. Claims 10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al (US Patent No. 5,239,639), Kim et al (US PGPub No. 20020054527), Schmitt (US Patent No. 5,587,675) and Sato et al (US Patent No. 5,946,251).

For claim 10, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose identifying the completion of the memory operation comprises detecting a bit line precharge enable signal transition indicating an initiation of a bit line precharge process.

Sato, however, discloses gate circuit drives read enable signal to the active state when bit line precharge instruction signal is at an inactive state and write enable signal is at an inactive state, indicating data reading; at the time of data reading, therefore, read enable signal is activated after the bit line precharge operation is completed (col. 13, lines 37-43).

Fischer, Kim, Schmitt and Sato are analogous art in that they are of the same field of endeavor, that is, a system and method for memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include identifying the completion of the memory operation comprises detecting a bit line precharge enable signal transition indicating an initiation of a bit line precharge process, because therefore, when the address signal and/or write enable signal makes transitions and designates writing or reading, a bit line precharge instruction signal activation allows for the precharging of a bit line to a prescribed potential level (col. 13, lines 52-56), as taught by Sato.

For claim 13, the combined teachings of Fischer, Kim, Schmitt and Sato disclose the invention as per rejection of claims 10 and 12 above.

These teachings further help disclose identifying the completion of the memory operation by identifying a transition of a bit line precharge enable signal, wherein the transition indicates an initiation of a bit line precharge process (Sato: col. 13, lines 37-43).

For claim 14, the combined teachings of Fischer, Kim, Schmitt and Sato disclose the invention as per rejection of claims 13 above.

These teachings further help disclose the predetermined time is sufficient to ensure that one or more true and complement bit line pairs substantially equalize and reach a predetermined precharge level (Fischer: col. 7 lines 7-15).

7. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al (US Patent No. 5,239,639), Kim et al (US PGPub No. 20020054527), Schmitt (US Patent No. 5,587,675) and Hovis et al (US Patent No. 6,434,082).

For claim 7, the combined teachings of Fischer, Kim and Schmitt disclose the invention as per the rejection of claim 6 above.

These teachings fail to disclose the predetermined time varies with respect to at least one of voltage, temperature and process condition variations.

Hovis, however, discloses a clocked memory device in which variations in process, voltage and temperature makes it difficult to start a precharge operation at the appropriate time without introducing unwanted delay (col. 4, lines 8-11).

Fischer, Kim, Schmitt and Hovis are analogous art in that they are of the same field of endeavor, that is, a clocked memory device for maximizing memory performance. It would have been obvious to a person of ordinary skill in the art at the time of the invention that predetermined time for such an operation would vary according to variations in process, voltage or temperature because the start of a precharge operation is usually accompanied unwanted delay (col. 4, lines 8-11), as taught by Hovis.

For claim 15. the combined teachings of Fischer, Kim, Schmitt and Hovis disclose the invention as per rejection of claims 7 and 14 above.

These teachings further help disclose the predetermined time varies with respect to at least one of voltage, temperature and process condition variations (Hovis: col. 4, lines 8-11).

8. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al (US Patent No. 5,239,639), Kim et al (US PGPub No. 20020054527), Schmitt (US Patent No. 5,587,675), Hovis et al (US Patent No. 6,434,082) and Sato et al (US Patent No. 5,946,251).

For claim 8, the combined teachings of Fischer, Kim, Schmitt and Hovis disclose the invention as per rejection of claim 7 above.

These teachings fail to disclose the variation in the predetermined time correlates substantially with a variation in time for the one or more true and complement bit line pairs substantially equalize and reach the predetermined precharge level due to variations in one or more of voltage, temperature and process conditions.

Sato, however, discloses a memory with bit line precharge/equalize circuits provided corresponding to respective bit line pairs and activated upon activation of a bit line equalize instruction signal for precharging and equalizing corresponding bit line pairs to a power supply voltage level (col. 1, lines 39-44) and that a specific level precharge potential level varies according to various conditions (col. 16, lines 6-7 and col. 15, lines 59-65).

Fischer, Kim, Schmitt, Hovis and Sato are analogous art in that they are of the same field of endeavor, that is, a system and method for memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention that variation in the predetermined time correlates substantially with a variation in time for the one or more true and complement bit line pairs substantially equalize and reach the

predetermined precharge level due to variations in voltage because the specific level precharge potential level is determined by factors such as the amount of current supplied from high resistance resistive elements in a memory cell, the degree of capacitance coupling between a bit line and a base electrode node, and the relation of the threshold voltages of access transistors when a back gate bias effect is caused (col. 15 lines 59-65), as taught by Sato.

For claim 16, the combined teachings of Fischer, Kim, Schmitt, Hovis and Sato disclose the invention as per rejection of claims 8 and 15 above.

These teachings further help disclose the variation in the predetermined time correlates substantially with a variation in time for the one or more true and complement bit line pairs substantially equalize and reach the predetermined precharge level due to variations in one or more of voltage, temperature and process conditions (Sato: col. 1, lines 39-44; col. 16, lines 6-7 and col. 15, lines 59-65).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Citation of Pertinent Prior Art

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hashimoto (US PGPub No. 20020097625) discloses a semiconductor memory device having a self refresh mode which may be entered in response to a self refresh set command and may be released in response to a self refresh release command.

Contact Information

11. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions

regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

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SCE 10/4/06

STEPHEN C. ELMORE
PRIMARY EXAMINER